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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/032,185	12/21/2001	Kenji Izumiya	01839/LH	4918

1933 7590 09/27/2005

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EXAMINER	
PHAM, HAI CHI	

ART UNIT	PAPER NUMBER
2861	

DATE MAILED: 09/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

. Office Action Summary	Application No.	Applicant(s)	
	10/032,185	IZUMIYA ET AL.	
	Examiner	Art Unit	
	Hai C. Pham	2861	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-6 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-6 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 21 December 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 9/24/02 & 9/8/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirasawa (U.S. 6,493,019) in view of Hanna (U.S. 6,259,467).

Hirasawa discloses an image forming apparatus having an image-writing section for forming an image of high precision with suppressed jitter of the video clock signal, the apparatus including a crystal oscillator (50, Fig. 10) for generating a reference clock signal (140), the jitter component included in the clock signal being suppressed by the jitter suppressing section, which divides the clock signal pulses (via 1/M frequency divider 702) to generate second dot clock pulses, and then, multiplies said second dot clock pulses to generate the video clock pulses (150) (the reference clock signal is first divided by the frequency divider 702 and the frequency-divided clock signal is multiplied

by the PLL consisting of the phase comparator 703, the low-pass filter 704, the voltage controlled oscillator 705 and the 1/N frequency divider 706).

Hirasawa fails to teach the digital-delay dot clock adjusting section.

Hanna discloses an image forming apparatus including a multi-tap delay line (330, Fig. 3B) to generate first dot clock pulses (alignment clock signal OSC2 322) having a predetermined number of pulses within a predetermined time interval at a constant exposing range of said image-writing section (e.g., the multi-tap delay having 10 taps producing a series of 10 pulses with separate taps separated by a fixed delay, the number of taps being necessary to cover the jitter coming out of the multi-tap delay line), wherein each period of said first dot clock pulses is slightly increased or reduced by changing a selection for a plurality of delayed clock pulses, which are generated by delaying clock-pulses, outputted from a reference oscillator (310), in slightly different delay times (the clock signal OSC2 having a fixed delay, however, the jitter would increase the period of the clock signal OSC2 as well as delay the clock signal OSC2 in different delay times as shown in Fig. 4A).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to incorporate the multi-tap delay line in the device of Hirasawa as taught by Hanna. The motivation for doing so would have been to achieve a better phase alignment of the dot clock with the beam detect pulse.

Hirasawa further teaches:

- The jitter suppressing section comprises a voltage controlled oscillator (705) to generate said second dot clock pulses (pulses having the frequency fout), a first

divider (1/M frequency divider 702), a second divider (1/N frequency divider 706) to divide said second dot clock pulses generated by said voltage controlled oscillator, and a phase comparator (703) to perform a frequency-phase comparison between first divided dot clock pulses outputted by said first divider and second divided dot clock pulses outputted by said second divider to output a comparison result voltage, and wherein said phase comparator feedbacks said comparison result voltage to said voltage controlled oscillator so as to constitute a phase locked loop, serving as a flywheel oscillator to disperse said jitter component (Fig. 10),

- The image-forming apparatus comprising an image-bearing member (scanning surface 38 of a photosensitive member) to bear a electrostatic latent image and/or a toner image on it, an image-writing device (laser source 81) to scan a surface of said image-bearing member with a scanning-light deflected by a rotating polygon mirror (83), a modulating section (laser driving unit 93 for modulating the light intensity of the laser source) that performs a pulse width modulation or a light-intensity modulation of dot clock pulses in response to image data to generate a scanning-light modulation signal to be fed to said image-writing device (Fig. 9), a developing section (not shown) that develops said electrostatic latent image, formed on said image-bearing member by said scanning-light, to form said toner image as a visual image, a transferring section (transfer belt 3) to transfer said toner image borne on said image-bearing member to a transfer material, a fixing section (not shown) to fix said toner

image, transferred to said transfer material, onto said transfer material (col. 5, line 56 to col. 6, line 4) (col. 6, lines 29-41),

- Said image-forming apparatus (Fig. 4) forms a color image based on a plurality of primary colors, and wherein said image-writing device (laser array 400) and said jitter suppressing section (PLL 51) are provided corresponding to each of said primary colors (Fig. 9).

4. Claims 3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hanna (U.S. 6,219,085) in view of Hirasawa.

Hanna ('085) discloses in Figs. 1 and 4 an electrophotographic printer for performing a duplex printing operation, the printer comprising a modulating section (beam modulator 22), a developing section (developer 17), a transferring section (transfer station 18), and a fixing section (not shown but inherently included in any electrophotographic printer) (col. 4, lines 12-46), a clock generating unit for generating a plurality of PEL clocks in which are provided a clock delay line (50) and a phase-locked-loop (PLL 67) for suppressing the jitter in the resulting PEL clocks and for finely adjusting the timing and/or size and length of each of the clocks to compensate for paper shrinkage, which occurs after printing the front size of the duplex-printed page so that printing on the back of the paper will be aligned with printing on the front (col. 5, lines 41-46).

Hanna ('085) fails to teach the jitter suppression section or PLL dividing the first dot clock signal to generate a second dot clock signal and then multiplying the second dot clock signal to generate the dot clock pulses.

Hirasawa discloses an image forming apparatus having an image-writing section for forming an image of high precision with suppressed jitter of the video clock signal, the apparatus including a crystal oscillator (50, Fig. 10) for generating a reference clock signal (140), the jitter component included in the clock signal being suppressed by the jitter suppressing section, which divides the clock signal pulses (via 1/M frequency divider 702) to generate second dot clock pulses, and then, multiplies said second dot clock pulses to generate the video clock pulses (150) (the reference clock signal is first divided by the frequency divider 702 and the frequency-divided clock signal is multiplied by the PLL consisting of the phase comparator 703, the low-pass filter 704, the voltage controlled oscillator 705 and the 1/N frequency divider 706).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify the PLL in the device of Hanna ('085) to include the first and second frequency dividers as taught by Hirasawa. The motivation for doing so would have been to provide the flexibility of varying the frequency dividing parameters, e.g., the N and M numbers, to adjust the frequency of the dot clock as well as to correct the main scan width as suggested by Hirasawa at col. 2, lines 28-30.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai C. Pham whose telephone number is (571) 272-2260. The examiner can normally be reached on M-F 8:30AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on (571) 272-1934. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hai C. Pham

HAI PHAM
PRIMARY EXAMINER

September 22, 2005